ABSTRACT OF THE DISCLOSURE

A scan synchronized frame buffer architecture includes a primary frame buffer implemented as part of a unified memory architecture (UMA) memory, and a secondary frame buffer implemented on a chipset/graphics component that is in communication with the UMA memory. When a pixel is changed in the primary frame buffer, that pixel is copied to the secondary frame buffer when the pixel is needed by the display. In particular, the pixel is transmitted simultaneously to a digital to analog converter and the secondary frame buffer, synchronized to the display refresh. This action mimics the effect the primary frame buffer would have on the display if the primary frame buffer were the actual frame buffer maintaining the display. Most of the bandwidth for maintaining display refresh is handled by the secondary frame buffer, returning substantially all of the bandwidth back to the UMA memory.